# American International University- Bangladesh
## Department of Electrical and Electronic Engineering
EEE 3102: Digital Electronics Laboratory

**Title: Derivation logic equations from a given engineering problem and implementation using CMOS technology**


**Abstract:**

This experiment is designed to-

1. Help students implement the logic circuits derived from a given statement using CMOS and observe whether the outputs satisfy the truth table of the given logic statement or not.
2. Perform relevant theoretical work for designing the logic circuit and truth table from the given logic statement and then simplify the equation using K-Map, De Morgan's Law and other Boolean algebraic operations to implement the circuit.


**Introduction:**

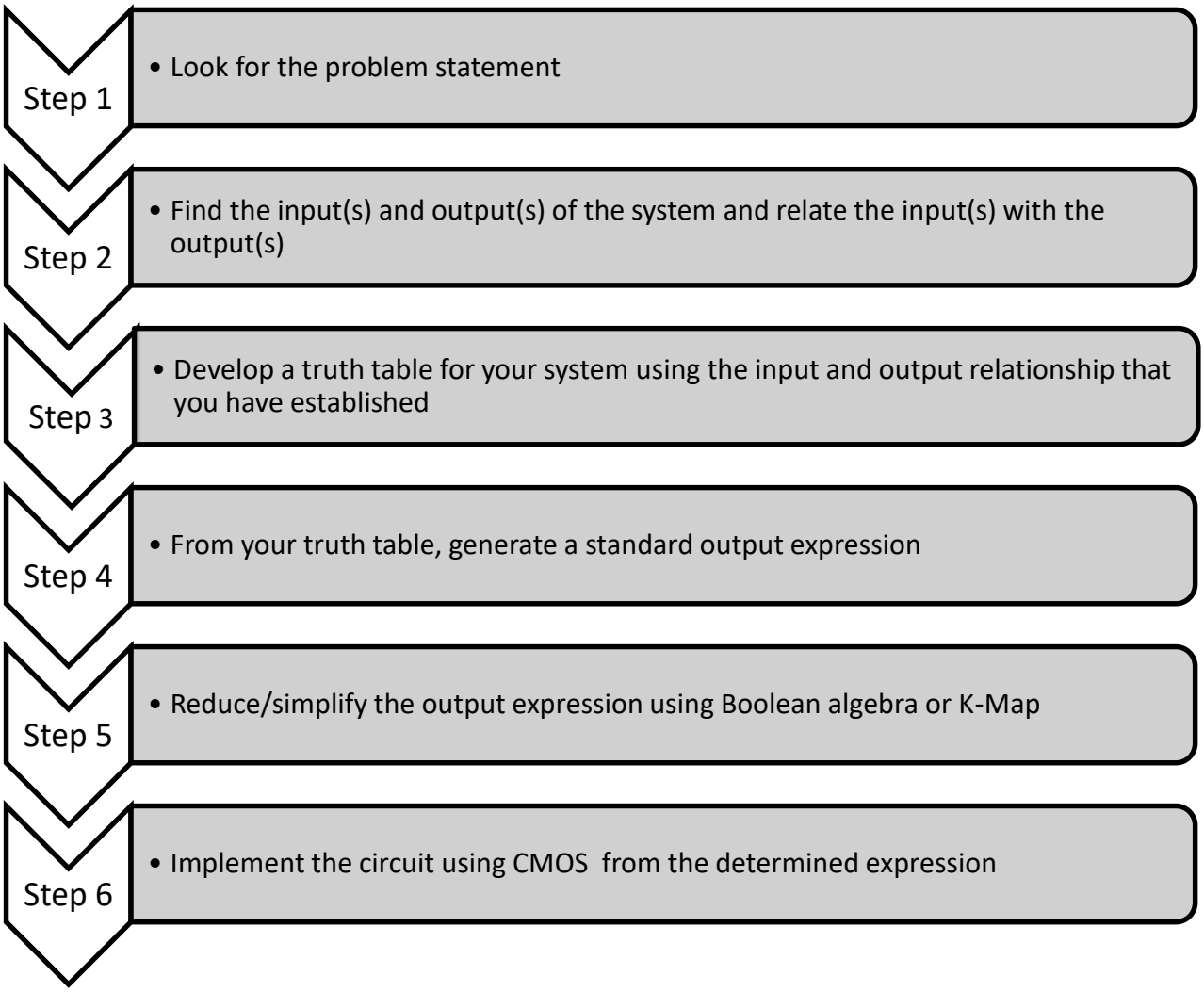
CMOS technology, which is mostly associated with the VLSI technology, is currently and has been presiding over the semiconductor industry for a good while now and scholars predict that this trend will continue at least for a few more years. There are several reasons for this technology to be so widely and resiliently popular. Firstly, CMOS technology is comparatively more reliable than contemporary technologies. Moreover, low power consumption and comparatively lower cost also play significant roles in making this the go-to technology for manufacturing ICs. However, one of the greatest appeals of CMOS is its scalability. Scalability refers to the ability of designing smaller and faster devices using a specific technology. Presently, VLSI devices integrate millions and sometimes billions of MOS transistors on to a single chip. The famous Gordon Moore observed the trends and predicted the doubling of the number of on-chip devices every 18-24 months whereas the size would be halved. For close to 50 years, this prediction has been sustained using CMOS technology. Today, MOSFET channel length has come down to 7nm and this has been possible due to the scaling ability in CMOS.

When it comes to digital CMOS circuits, the relationship between a logic statement and a logic circuit runs quite deep. From any given logic statement, it is possible to construct a digital logic circuit. The first step in this process is to construct a truth table and then determine a standard SOP (sum of products) or POS (product of sums). Conversely, it is also possible to derive a logic expression from a given combinational circuit diagram by observing the individual logic operations performed in the circuit and matching them with their corresponding logic gates. Expressions are simplified using Boolean algebra and De Morgan's law or K-Map which also helps to reduce the number of gates used in the circuit. Then the circuit is implemented in the breadboard using CMOS and observed whether the output satisfies the truth table of the given statement.

This experiment gives the students a basic idea about how to derive logic equations and truth tables from combinational circuits. Not only does this train the students to solve any logic circuits, but also aids them in relating real life problems with in-book theories.

## Theory and Methodology:

Combinational circuits consist of logic gates and other necessary components. The main feature of this family of circuits is that the output depends on the present state of the circuit only and not any of the previous states. This also implies that combination circuits don't have any memory elements. A combination digital system is commonly designed using the following steps:




## Experimental Problems:

**Problem 1:** In a bank, there are four employees. They are the bank manager, assistant manager, teller and the security guard. The bank has a single vault to store money. This vault was designed such that it needs four signals to open it. These four signals are from the four employees. For the vault to open, it needs to satisfy all of the following conditions:

1. No single employee can open the vault.
2. Can be opened with three employees which includes the manager
3. Can be opened by the manager together with the assistant manager.

We want to design a logic circuit that will automatically open the vault if these conditions are met.

**Solution:**

**Representation of Logic**: In logic circuit, we used only the logic 1 and 0. For this, we will assign the following logic to open and close.

- Logic 1 = Open
- Logic 0 = Close

**Writing the formula of the function**: We will assign symbols for the logic of the employees;

- A= Manager (Logic 1 = A , Logic 0 =$\overline{A}$)
- B= Assistant manager (Logic 1 = B , Logic 0 = $\overline{B}$)
- C= Teller (Logic 1 = C , Logic 0 = $\overline{C}$)
- D= Security Guard (Logic 1 = D, Logic 0 = $\overline{D}$)

For this, we will consider the logic for opening the vault is 1. From the above conditions, we will formulate every functions that would result to Logic 1 or opening of vault. So, for the second condition, the vault will open if three employees including the manager put their signals in. Here are the functions to achieve logic 1:

- $A\overline{B}CD$= (assistant manager did not open)
- $AB\overline{C}D$ = (teller did not open)
- $ABC\overline{D}$ = (security guard did not open)
- ABCD = (all employees open it)

The third condition states that the vault can be opened by the manager together with assistant manager. Here is the function:

- $AB\overline{CD}$= (teller and security guard did not open)

**The complete function that will open the vault based on the given conditions is;**

**f(A,B,C,D) =** $A\overline{B}CD$ + $AB\overline{C}D$ + $ABC\overline{D}$ + ABCD + $AB\overline{CD}$

Using our knowledge of Boolean algebra, we will simplify the function equation. Simplification of the equation will get rid of redundant terms and thus fewer logic gates will need to be used to make our circuit. This will also make the truth table more compact.

**Simplifying process**

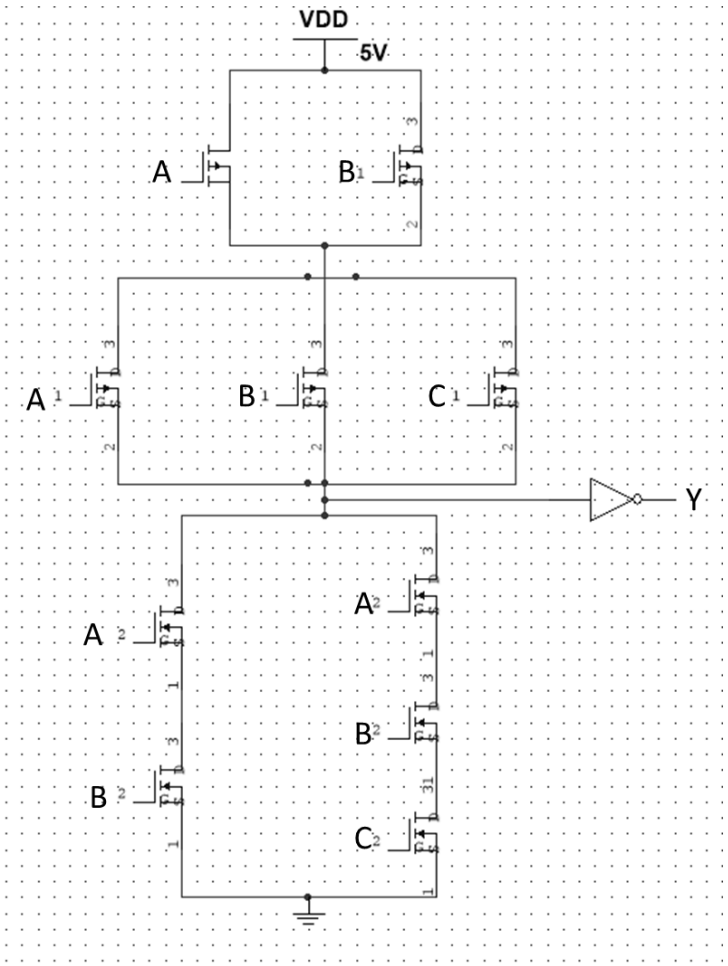
- f(A,B,C,D) = $A\overline{B}CD$+ $AB\overline{C}D$+ $ABC\overline{D}$ + ABCD + $AB\overline{CD}$
  = $A\overline{B}CD$ + AB ($\overline{C}D$ + $C\overline{D}$+ CD + $\overline{CD}$)
  = $A\overline{B}CD$ + AB [$\overline{C}$(D + $\overline{D}$) + C(D + $\overline{D}$)]
  = $A\overline{B}CD$ + AB($\overline{C}$+ C)
  = $A\overline{B}CD$ + AB
  = ACD + AB [As, A + $\bar{A}$B = A + B]

**So, simplified equation is: f (A, B, C, D) =** ACD + AB

**Truth table:**

| A | B | C | D | Y |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Circuit Diagram:**



**Problem 2:** In a simple copy machine, a stop signal S is to be generated to stop the machine's operation and light up the indicator light whenever either of the following condition are met:

1. There is no paper in the paper feeder tray.

Or,

2. The two micro switches in the paper path are activated, indicating the paper path being jammed.

The presence of paper in the feeder paper tray is indicated by a HIGH at logic signal P. Each of the micro switches produces a logic signal (Q&R) that goes to HIGH whenever a paper is passing over the switches to activate it. Design a logic circuit that produces high logic outputs for the given conditions.

**Solution:** Use solution technique from **Problem 1** to solve the statement.

## Pre-Lab Homework:

1) Derive De Morgan's union and intersection laws and transform the set equation into Boolean algebraic equations.
2) Verify the transformed equations using necessary truth tables.

## Apparatus:

1.Digital trainer board
2.IC 7404 (Inverter)
3.PMOS
4.NMOS
5.Connecting wires

**Precaution:** Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within VDD) to turn on the transistors and/or chip, otherwise they may get damaged.

## Experimental Procedure:

a) Solve the given engineering problem and determine the logical expression for the output.
b) Make a Truth table from the determined expression.
c) Implement the circuit using CMOS technology.
d) Verify the results with Truth table values.

## Simulation and Measurement:

Compare the simulation results with your experimental data and comment on the differences if any.

## Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

**Report Questions:**

**ABC+ A'B'C+ A'BC'+AB'C'**

Design the transistor level circuit for this equation. Analyze and then identify the circuit. Mention how this circuit can be used in performing arithmetic operations with necessary circuits and validate your answer.

**References:**

1. Thomas L. Floyd, "Digital Fundamentals", available Edition, Prentice Hall International Inc.
2. Link : https://steemit.com/cn/@thinkingmind/how-to-give-solution-to-a-problem-using-logic-circuit
3. Link: https://www.docsity.com/en/design-problem-nand-and-gates-digital-logic-design assignment/170781/